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Anisotropic layer-by-layer growth of graphene on vicinal SiC(0001) surfaces

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Epitaxial graphene is formed on vicinal SiC(0001) surfaces via high temperature annealing in vacuum. Steps act as a significant "kicker" of graphene nucleation to feed C atoms. At elevated temperatures, graphene growth is controlled by the decomposition of Si-C bonds at step edges, Si desorption, and C diffusion on the surface. The limited Si desorption is due to the dependence of the growth rate on the thickness of graphene layers. The fabricated graphene layer(s) acts as a Si-diffusion barrier, which in turn induces local thermal equilibrium between the graphene layer and the SiC surface. C atoms preferentially diffuse along the steps, resulting in anisotropic layer-by-layer growth, which is characteristic in this system.

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Experimentalists who pursue developments in condensed matter physics and next-generation nanoelectronic devices consider graphene to be very significant since it is an excellent two-dimensional substance used in experiments with table-top setups. After the successful fabrication of graphene by the mechanical exfoliation method,[1] there have been several significant studies using tiny pieces of graphene flakes in various fields such as pure condensed matter physics and in the development of various device applications.[2–4] For future applications and further simplification of the experiments, it is essential to scale up the size and to increase the stability of the crystal quality of these flakes. The surface modification of silicon carbide (SiC) substrates in vacuum is one of the promising approaches for fabricating epitaxial graphene;[5–7] this method is as simple as mechanical exfoliation and can potentially be used for producing graphene of enhanced size and stable crystal quality. In the future, it will be possible to fabricate single layer graphene and a few layers of graphene (FLG) over the entire surface of the SiC substrate. Presently, however, there are several problems in this process, related to structural and electrical properties such as spatial thickness variation,[8] domain sizes,[9] rotational domains,[10] surface morphology,[11] low-carrier mobility,[12] etc. These problems still need to be investigated and resolved. The work of Emtsev *et al.* resulted in a significant development, when they demonstrated the fabrication of monolayer graphene with sufficiently large domain sizes on SiC substrates by high temperature annealing in an Ar atmosphere and nearly atmospheric pressure.[12] This suggests that thermal equilibrium conditions result in a better quality of graphene in terms of thickness variation and crystal perfection.[13] It should be noted that most studies on epitaxial graphene have used on-axis SiC(0001) substrates although these substrates contain surface steps due to unintentional miscuts of the substrate. The significance of surface steps in understanding modulated surface morphologies,[14] step edge instabilities,[15] and pit formation[9] has been discussed in earlier studies. Very few papers discussed vicinal SiC surfaces (typically off-cut by 3.5° and 8°) probably due to difficulties in control growth and structural analyses.[16,17]

We have studied vicinal SiC surfaces that are intentionally off-cut from a (0001) plane and have observed a unique surface structural ordering on the nanometer scale.[18] After a high-temperature H_2-gas etching, the vicinal SiC surfaces underwent surface phase separation, quantized step bunching, and ordering, and exhibited self-ordered nanofacet structures consisting of pairs of a (0001) basal plane and a $(11\bar{2}n)$ nanofacet with a characteristic distance of 10/20 nm,[19] depending on the polytype and the etching temperature. Such unique vicinal SiC surfaces would play a significant role in obtaining spatially uniform graphene layers and contributing to crystal quality. It is very difficult to reproduce similar periodic features run-to-run (periodicity and step direction) on the on-axis substrate due to unintentional miscuts (e.g., $<0.2°$) in unknown directions.

Initially, vicinal 6H-SiC substrates (Si-face, 4° off toward $[11\bar{2}0]$) underwent H_2-gas etching, followed by N_2 annealing under atmospheric pressure. N_2 annealing energetically stabilizes the nanofacet surfaces by introducing epitaxial SiON superlattices,[20] which exhibit a $(\sqrt{3}\times\sqrt{3})$R30° surface reconstruction even after exposure to the air. The resultant SiC samples were then loaded into an ultra-high-vacuum chamber and were heated by direct current to the temperatures at 1250 °C ~ 1600 °C, keeping the pressure below 2×10^{-9} Torr. The samples were then investigated *ex situ* by several techniques such as atomic force microscopy (AFM), low-energy electron microscopy (LEEM), high-resolution transmission electron microscopy (HRTEM), micro-Raman spectroscopy, and angle-resolved photoemission spectroscopy (ARPES). In this study, we especially focus on growth mechanisms by means of spatial thickness evolution as observed using LEEM. The physical properties of these samples will be reported elsewhere.

Figures 1(a)–1(c) show AFM images of the samples before and after surface graphitization at 1400 °C for 30 min and at 1600 °C for 10 min. After being etched by H_2 gas, the starting SiC surface clearly indicates a periodic structure with the distance of ~20 nm, consisting of pairs of a (0001) basal plane and a $(11\bar{2}n)$ nanofacet. This surface morphology was modulated after the graphitization process; bunched and wandering steps were observed on the surface, and, importantly, pits or voids were not observed. Pits or voids on the nanometer scale are often observed in graphene grown on on-axis SiC surfaces; these pits or voids are formed due to Si evaporation on the terraces followed by preferential nucle-

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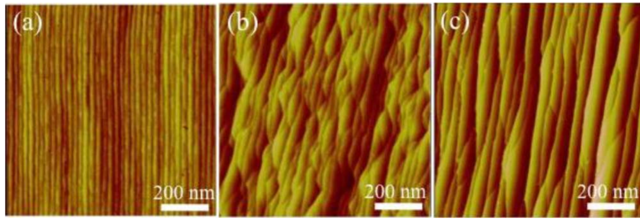

FIG. 1. (Color online) AFM images of the samples (a) before surface graphitization, (b) after surface graphitization at 1400 °C for 30 min, and (c) after surface graphitization at 1600 °C for 10 min. After H_2-gas etching, a well-ordered nanofacet structure with a periodicity of ~20 nm is clearly observed in (a). After annealing the surface, the morphologies are degraded due to step bunching and wandering.

ation of graphene.[8,9] Hence, the use of vicinal SiC surfaces provides this significant advantage over the use of on-axis substrates.

Each graphene sample was characterized by LEEM to evaluate spatial thickness distribution.[8] Figures 2(a)–2(c) show bright-field (BF)-LEEM images of the sample annealed at 1250 °C, 1400 °C, and 1600 °C, respectively, where monolayer, bilayer, trilayer, and quadralayer graphenes are clearly discernible owing to the difference in the electron reflectivity. The sample annealed at 1250 °C contains very fine and dense structures that hinder a proper observation of the spatial thickness distribution. Although the average layer thickness of the samples annealed at 1400 °C for 600 s and 1600 °C for 600 s is approximately the same [~2.3 monolayer (ML)], the spatial distribution of the layer thickness, as well as the surface morphology, is different. The higher-annealing temperature can improve the thickness distribution and the surface morphology. Moreover, it should be noted that the thicker regions (3 ML) are spaced along the step direction, perpendicular to $[11\bar{2}0]$, and are more elongated for the samples annealed at 1600 °C. Nucleation of graphene starts in the vicinity of nanofacet regions consisting of steps[8,9] and lateral growth via layer-by-layer mode essentially takes place along the step direction, resulting in anisotropic layer-by-layer growth. This feature is probably due to the enhanced diffusion length of C atoms, as will be discussed later.

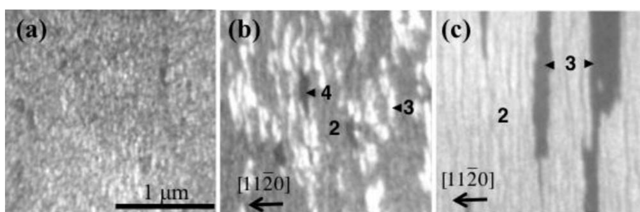

FIG. 2. LEEM images of graphene layers annealed at (a) 1250 °C for 1800 s, (b) 1400 °C for 600 s, and (c) 1600 °C for 600 s. The electron beam energies are (a)(b) 3.5 and (c) 3.0 eV. The numerals in the figures indicate the layer thickness of graphene. The sample annealed at 1250 °C in (a) contains very fine structures that hinder a proper observation of the spatial thickness distribution. Each figure has the same magnification, as shown by the scale bar in (a).

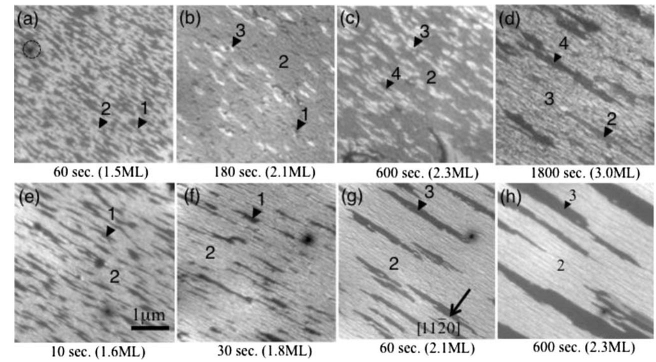

FIG. 3. LEEM images of graphene layers annealed at (a)(d) 1400 °C and (e)(h) 1600 °C for various time durations. The electron beam energies are (a)–(d) 3.5 and (e)–(h) 3.0 eV. The average layer thickness is indicated below each figure. Each figure has the same magnification as indicated in (e) and step direction as indicated in (g).

We attempted to understand the growth mechanism of graphene layers by investigating the time evolution of the spatial thickness distribution at 1400 °C and 1600 °C. Figures 3(a)–3(h) show the BF-LEEM images at 1400 °C (upper row) and 1600 °C (lower row) as functions of the annealing time and average thickness calculated using the areal ratio of each thickness (in ML). Two significantly different features are recognized between the samples annealed at 1400 °C and those at 1600 °C—the degree of spatial thickness distribution and anisotropy in graphene growth directions. The former can be clearly observed by comparing the samples. For example, observe the samples shown in Figs. 3(b) and 3(g), having the same average thickness of 2.1 ML. The samples annealed at 1400 °C exhibit segments with a thickness of 1 ML (in dark gray) and 3 ML (in white) embedded in a 2 ML matrix whereas the samples annealed at 1600 °C exhibit elongated 3 ML islands in a 2 ML matrix due to anisotropic layer-by-layer growth. These features can be understood by considering C diffusion kinetics at the graphene/SiC interface.

The average layer thickness is plotted as a function of the annealing time in Figs. 4(a) and 4(b). As the annealing time is increased, the layer thickness increases nonlinearly. Even though the time scale is different at each temperature, the pattern of growth rate is similar: very high-growth rate in the initial stage up to a thickness of ~1 ML and dramatically reduced growth rates in the following stages. This pattern suggests that the growth rate is limited by the graphene layer thickness. Here, three stages can be considered, as shown in Fig. 5. Stage I (0–1 ML) consists of the formation of the $(6\sqrt{3}\times 6\sqrt{3})R30°$ buffer layer[21] and nucleation of 1 ML graphene at the nanofacets, followed by 1 ML graphene growth over the entire surface. Stage II (1–2 ML) consists of the nucleation of the second graphene layer at the nanofacets below the first graphene layer and a continuous graphene growth via layer-by-layer mode. Stage III (2–3 ML) is similar to stage II in all respects except that the graphene thickness has increased. The growth rate at each stage is calculated and shown in Fig. 4. One could be puzzled by the lower growth rate at 1600 °C than at 1400 °C assuming a ther-

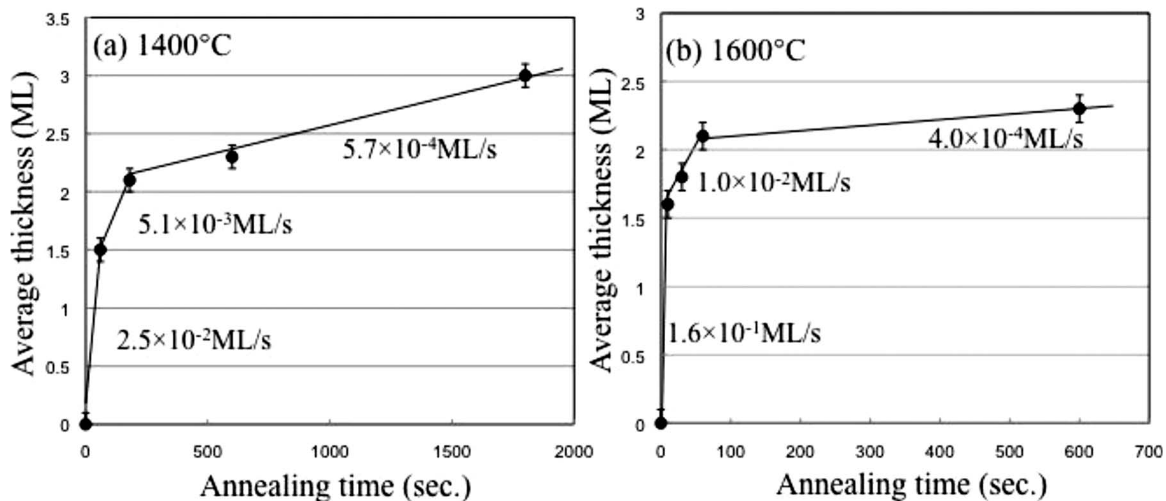

FIG. 4. Average layer thickness of graphene for various annealing time durations at (a) 1400 °C and (b) 1600 °C. Note the stepwise decrease in growth rate with the increase in the graphene layer thickness. The growth rates (ML/s) at the stage I, II, and III are also shown.

mally activated process. This might be related to the quality of the top graphene layer, which is inferior in quality grown at 1400 °C where Si desorption more likely occurs through defects as will be explained in the following paragraph. In stage I, the step edges at the nanofacets are unstable at elevated temperatures and start to decompose and release Si and C atoms. Si atoms are desorbed from the surface, and C atoms migrate on the surface. This process takes place continually until the surface is covered by the $(6\sqrt{3}\times6\sqrt{3})R30°$ buffer layer.[8] It is not known whether the same buffer layer is present at the nanofacet area at this moment. C atoms released at the nanofacet area can then be clustered in order to nucleate graphene. This is followed by lateral growth of graphene via layer-by-layer mode to complete fabrication of 1-ML-thick graphene. Then, nucleation of the second graphene layer occurs at the nanofacet sites below the first graphene layer,[22] where there are still step edges to be decomposed. From the reduced growth rate in stage II, we can infer that the overgrown graphene layer acts as a Si-diffusion barrier, hindering Si desorption from the surface. Thus, nearly thermal equilibrium conditions may be created between the graphene layer and the SiC surface. These conditions may affect the crystal quality of graphene as suggested by the work of Emtsev *et al.*[12] In stage III, an even reduced growth rate indicates higher-diffusion barriers for Si desorption from the SiC surface, owing to two graphene layers on top.

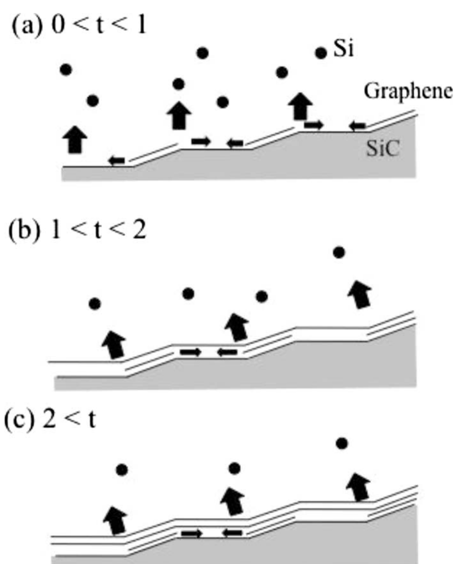

FIG. 5. Schematic models of graphene growth at each stage. (a) Stage I: 0 to 1 ML via the $(6\sqrt{3}\times6\sqrt{3})R30°$ buffer layer (not shown), (b) stage II: 1 to 2 ML, and (c) Stage III: 2 to 3 ML. An overgrown graphene layer(s) acts as a diffusion barrier for the Si desorption, resulting in the decrease in growth rates.

The LEEM image in Fig. 3(g) shows stripe-like islands of the third graphene layer (in gray) grown via anisotropic layer-by-layer growth. It should be noted that the nucleation density is reduced as compared to that of stage II and that growth perpendicular to the step edges is enhanced. This enhancement in the growth leads to a coalescence of the stripelike islands as observed in Fig. 3(h). Since the free C atoms produced solely at the nanofacets diffuse to the nuclei along the step edges, growth via anisotropic layer-by-layer mode is achieved. The C diffusion perpendicular to the step edges toward the terrace regions may be energetically difficult initially but complete parallel growth via anisotropic layer-by-layer mode results in long stripes causing the C atoms to overflow to terrace regions. Energies of such diffusion barriers should be studied on the basis of theoretical approaches. This anisotropic layer-by-layer growth is characteristic of graphene growth on SiC nanofacet surfaces. At lower annealing temperature, the C diffusions parallel and perpendicular to the nanofacets are suppressed, resulting in the higher density of islands.

The Si desorption from the surface/interface is the key process at all stages. As the growth rate decreases with the increasing graphene thickness, it can be hypothesized that the Si desorption through the graphene layer(s), i.e., the Si out-diffusion, limits the growth process. The Si out-diffusion path is not identified yet; however, it is probably dominated

by the structural defects induced in graphene layers, such as point defects[22] and domain boundaries.[10] Dark-field (DF) LEEM imaging using (01) and (10) diffraction beams can be used to visualize inversion domains. These inversion domains are typically observed in FLG (>2 ML) on on-axis SiC(0001) substrates where a clear contrast inversion is observed between the (10) and (01) DF imaging condition.[10] The DF-LEEM images of the samples used in this study (not shown), however, showed very fine contrast modulation and no clear contrast inversion. Presently, we cannot identify the nature of the contrast, which may be due to local change in diffraction conditions caused by strains. More detailed investigations will be reported using quantitative LEED and scanning tunneling microscopy (STM).

In summary, we have investigated graphene growth on vicinal SiC(0001) surfaces consisting of ordered nanofacets structures. The step edges at the nanofacet regions are easily decomposed and supply C atoms to nucleate graphene at elevated temperatures. The growth proceeds in layer-by-layer mode along step edges, i.e., anisotropic layer-by-layer growth. The growth rate dependence on graphene thickness is indicative of the Si desorption (out-diffusion) limited process. The grown graphene layer(s) acts as a Si-diffusion barrier and creates thermal equilibrium conditions, which is probably a key factor in achieving graphene layers with a high-crystal quality.

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